ABSTRACT

An FEC multiplexing circuit (2) has a configuration in which a first memory circuit (15) is arranged on the input stage of a first RS encoding circuit (16), a second memory circuit (17) is arranged on the input stage of a second RS encoding circuit (18), error correction encoding is performed by a combination of different data having two directions, and thereafter, error correction codes are multiplexed to generate an FEC frame. On the other hand, an FEC demultiplexing circuit (6) has a configuration in which a third memory circuit (42) is arranged on the output stage of a first RS decoding circuit (41), a fourth memory circuit (44) is arranged on the output stage of a second RS decoding circuit (43), error correction is performed by a combination of different data having two directions, and, thereafter, parallel data read from the fourth memory circuit (44) are multiplexed to reproduce original information data.